REMARKS

Claims 1-16 are pending in the present application. Claims 17-22 have been canceled as being directed to a non-elected invention. Applicants respectfully reserve the right to file a divisional application including non-elected claims 17-22.

The specification and claims have been amended to change "inequity" to "inequality" and to improve antecedent. Since the amendments to the claims are merely for the purpose of improving accuracy and not for the purpose of further distinguishing the claims over prior art, the amendments to the claims should not be construed as narrowing scope within the meaning of *Festo*.

Priority Under 35 U.S.C. 119

Japanese priority application 2000-104733 has been filed concurrently herewith in a separate letter. **The Examiner is respectfully requested to acknowledge receipt of the priority document and that the claim for priority under 35 U.S.C. 119 is now complete.**

Conclusion

Favorable consideration and early allowance of the present application are earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581)

at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:cej

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Version with marked-up changes

Serial No. 09/825,973

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Abstract:

A field effect transistor having metallic silicide layers is formed in a semiconductor layer on an insulating layer of an SOI substrate. The metallic silicide layers are composed of refractory metal and silicon. The metallic silicide layers extend to bottom surfaces of [a] source and [a] drain regions. A ratio of the metal to the silicon in the metallic silicide layers is X to Y. A ratio of the metal to the silicon of metallic silicide having the lowest resistance among [stoichiometaric] stoichiometric metallic silicides is X0 to Y0. X, Y, X0 and Y0 satisfy the following [inequity] inequality: (X / Y) > (X0 / Y0).

Additions/Deletions to the Specification:

Page 4, lines 6-12:

In order to achieve the above object, in a field effect transistor having metallic silicide layers composed of refractory metal and silicon[. Wherein], the bottom surfaces of the metallic silicide layers respectively extend to the bottom surfaces of a semiconductor layer[. Wherein], wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among [stoichiometaric] stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following [inequity] inequality: (X / Y) > (X0 /

Y0).

Page 7, line 7 through to page 8, line 4:

The source and the drain regions excepting the highly-doped silicon impurity layers 8a and 8b are comprised of metallic silicide layers 9a and 9b. The metallic silicide layers 9a and 9b are composed of refractory metal and silicon. An amount of refractory metal contained in the metallic silicide layers 9a and 9b is more than that of silicon. In the first preferred embodiment, the metallic silicide layers 9a and 9b are comprised of a CoSiz layer in which a ratio of cobalt to silicon is one to z (1<z<2). In other words, a ratio of metal to silicon in the metallic silicide layer is X to Y, a ratio of metal to silicon of metallic silicide having the lowest resistance among [stoichiometaric] stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following [inequity] inequality: (X / Y) > (X0 / Y0). The CoSiz layers 9a and 9b are formed by a conventional silicide process, for more detail, all of the source region and the drain region except under the sidewalls 7a and 7b are changed into the cobalt silicide layers 9a and 9b. That is, bottom surfaces of the cobalt silicide layers 9a and 9b extend to bottom surfaces of the SOI layer 3. An electrical connection between the CoSiz layers 9a and 9b and the SOI layer 3 is performed between the highly doped silicon layers 8a and 8b and the CoSiz layers 9a and 9b only.

Additions/Deletions to the Claims:

1. (Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions [where] which are respectively in contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein bottom surfaces of the pair of metallic silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among [stoichiometaric] stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following [inequity] inequality:

(X / Y) > (X0 / Y0).

5. (Amended) A field effect transistor including a gate electrode and a channel

region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region defined by the source region and the drain region;

a pair of impurity layers formed into regions [where] <u>which</u> are respectively <u>in</u> contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively <u>in</u> contact with the pair of impurity layers, wherein the pair of metallic silicide layers have a thickness which is equal to or more than 80% thickness of from the upper surface of the metallic silicide layers to the bottom surface of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among [stoichiometaric] <u>stoichiometric</u> metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following [inequity] <u>inequality</u>:

$(X / Y) > (X0 / Y0)$.

9. (Amended) A field effect transistor formed in a semiconductor layer located

on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first impurity layer and the first metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second impurity layer and the second metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity [region] <u>layer</u> and the second impurity <u>layer</u>,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among [stoichiometaric] <u>stoichiometric</u> metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following [inequity] <u>inequality</u>:

$(X / Y) > (X0 / Y0)$.

13. (Amended) A field effect transistor formed in a semiconductor layer located

on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first metallic silicide layer [have] has a thickness which is equal to or more than 80% a thickness of from [the] an upper surface of the first metallic silicide layer to [the] a bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second metallic silicide layer [have] has a thickness which is equal to or more than 80% a thickness of from [the] an upper surface of the second metallic silicide layer to [the] a bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity [region] layer and the second impurity layer,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among [stoichiometaric] stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following [inequity] inequality:

$(X / Y) > (X0 / Y0)$.